

FIG. 1

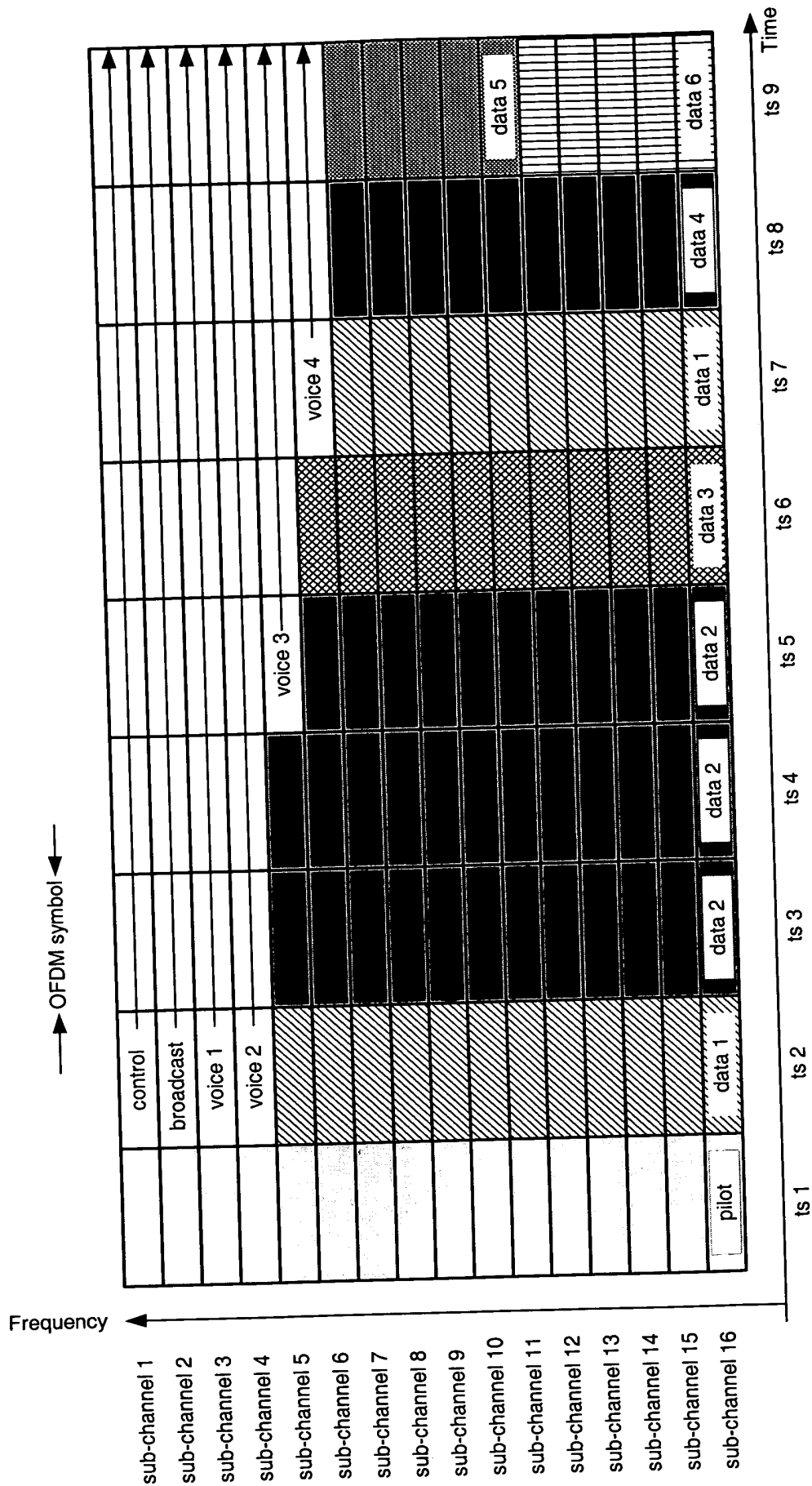


FIG. 2

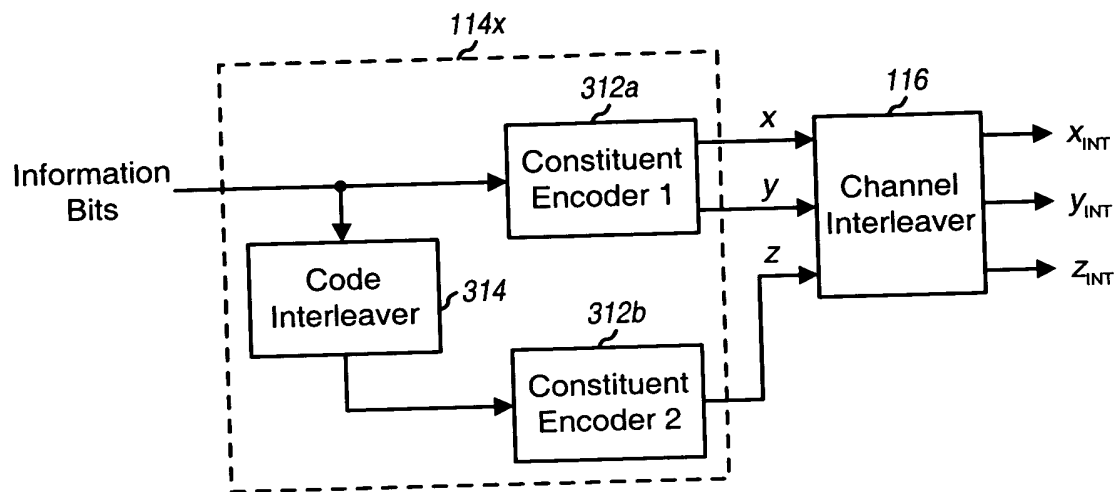


FIG. 3A

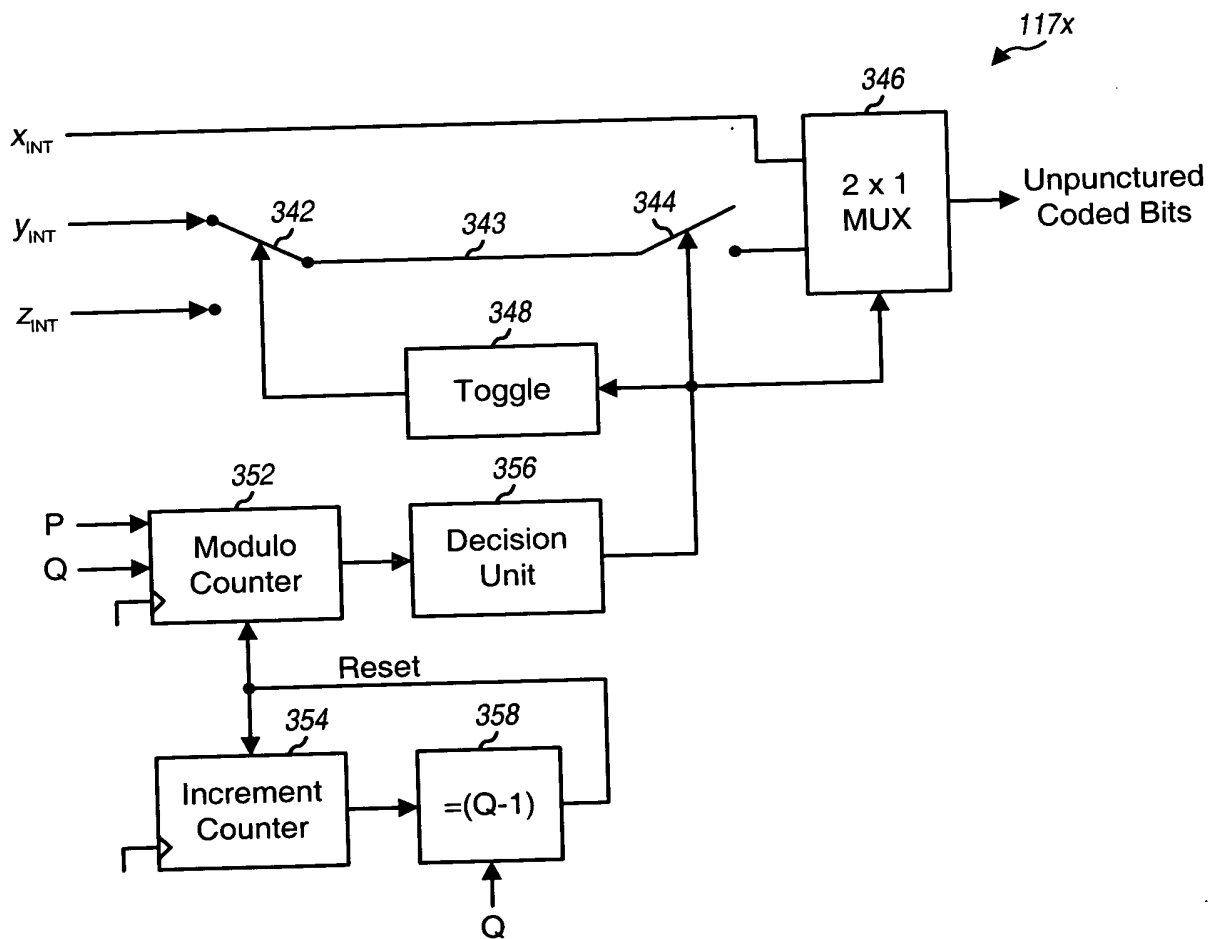
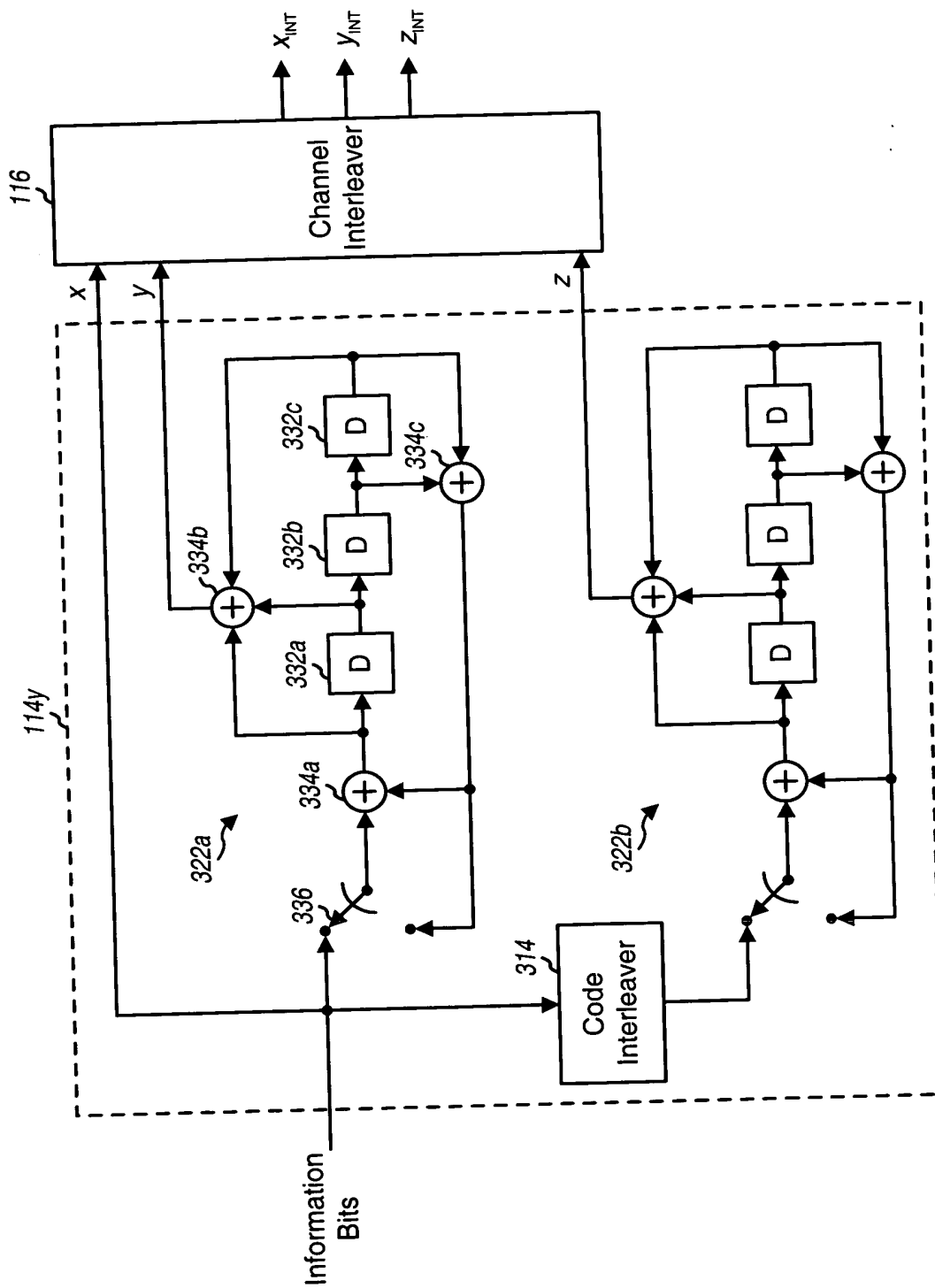
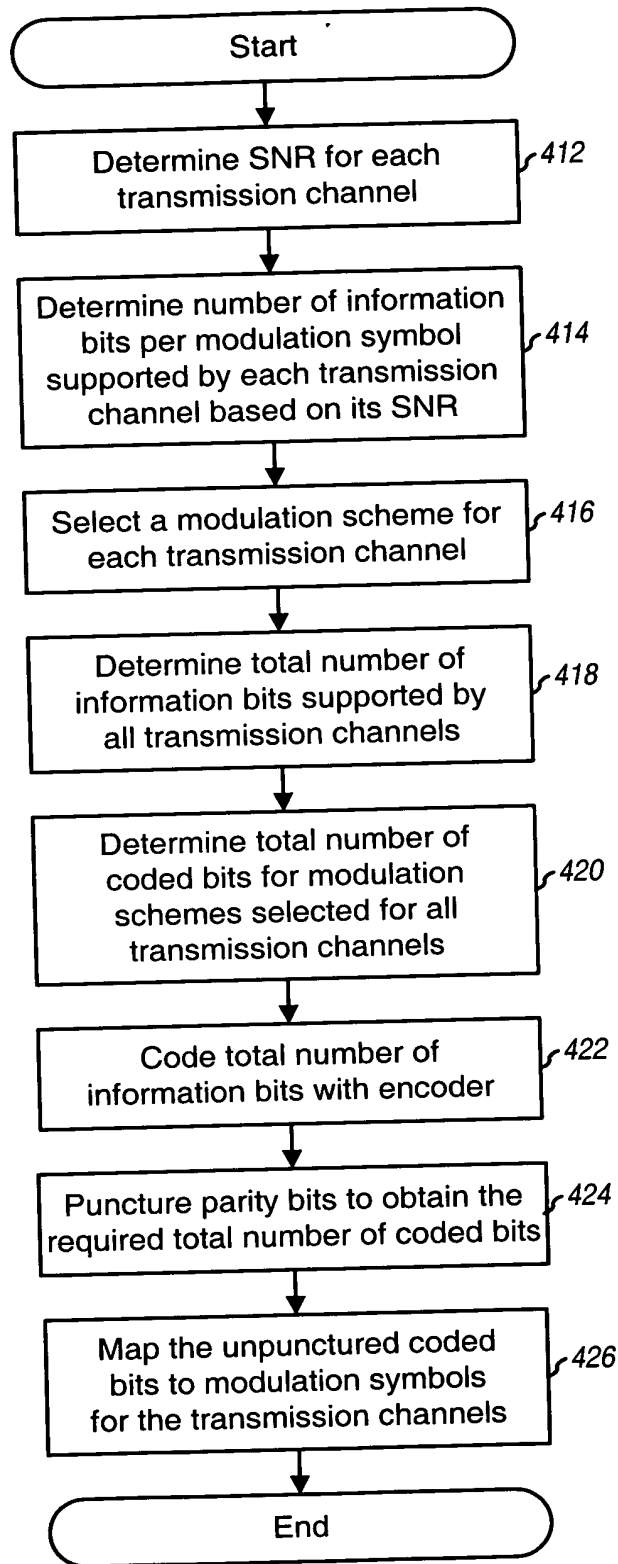
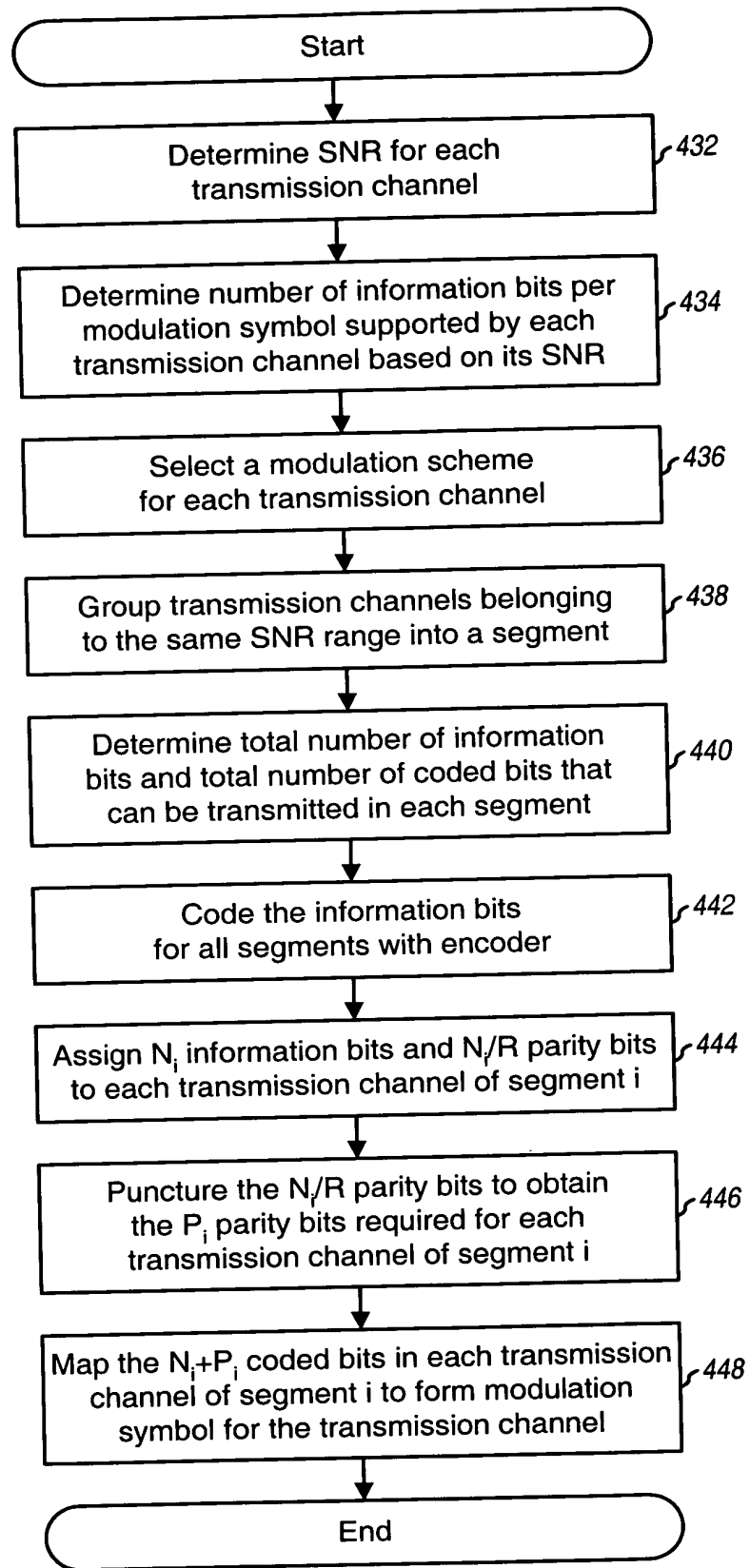


FIG. 3C

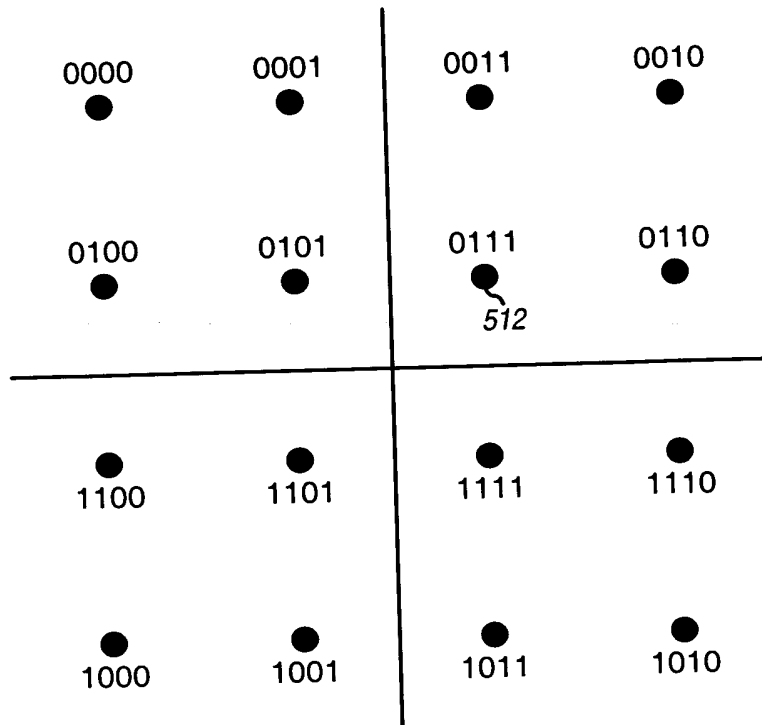




**FIG. 4A**



**FIG. 4B**



**FIG. 5**

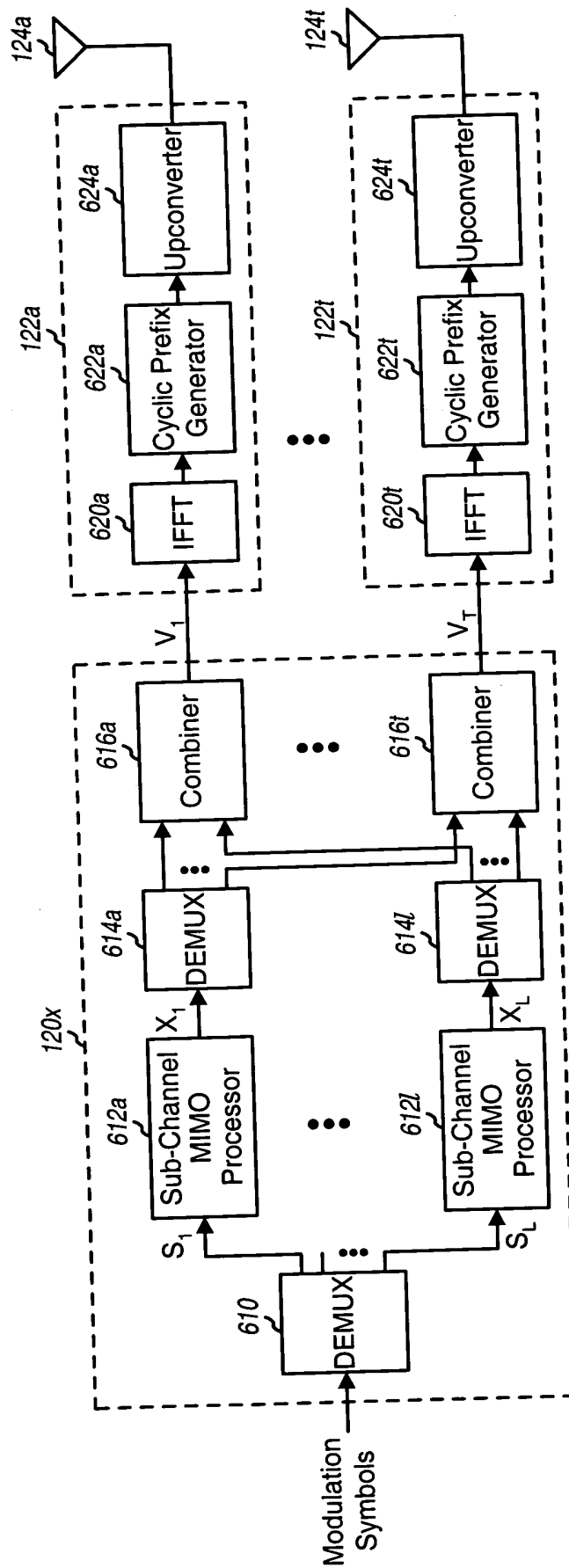


FIG. 6



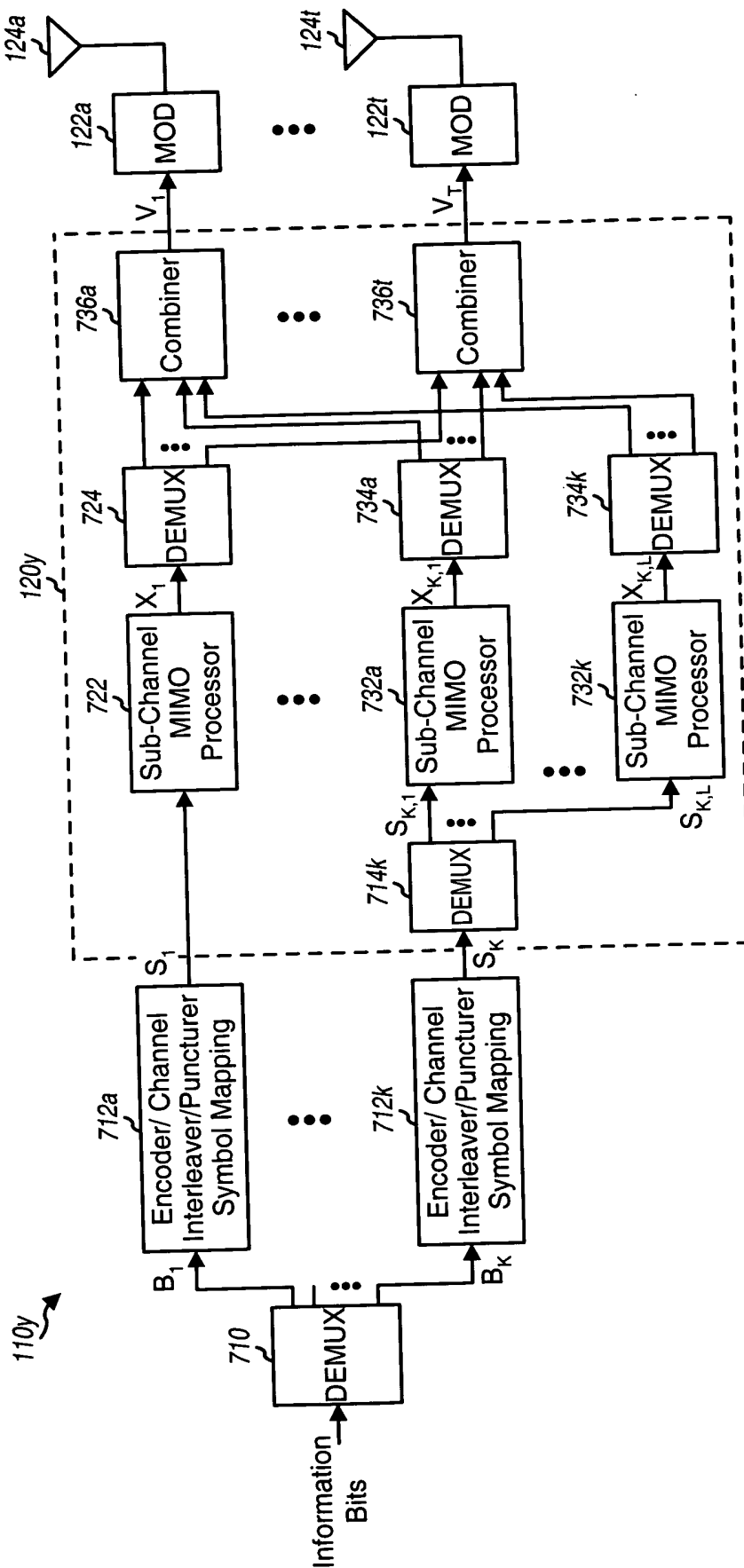


FIG. 7

FIG. 8 is a block diagram of a receiver system 162x, which includes a Bit LLR Calculation block 158x, a De-Puncturer block 159, a Channel Deinterleaver block 160, and a Detector block 818. The system also includes a feedback loop with a Code Interleaver block 814, a Decoder block 812a, a Decoder block 812b, and a Code Deinterleaver block 816. The system processes Received Modulation Symbols to produce Decoded Bits.

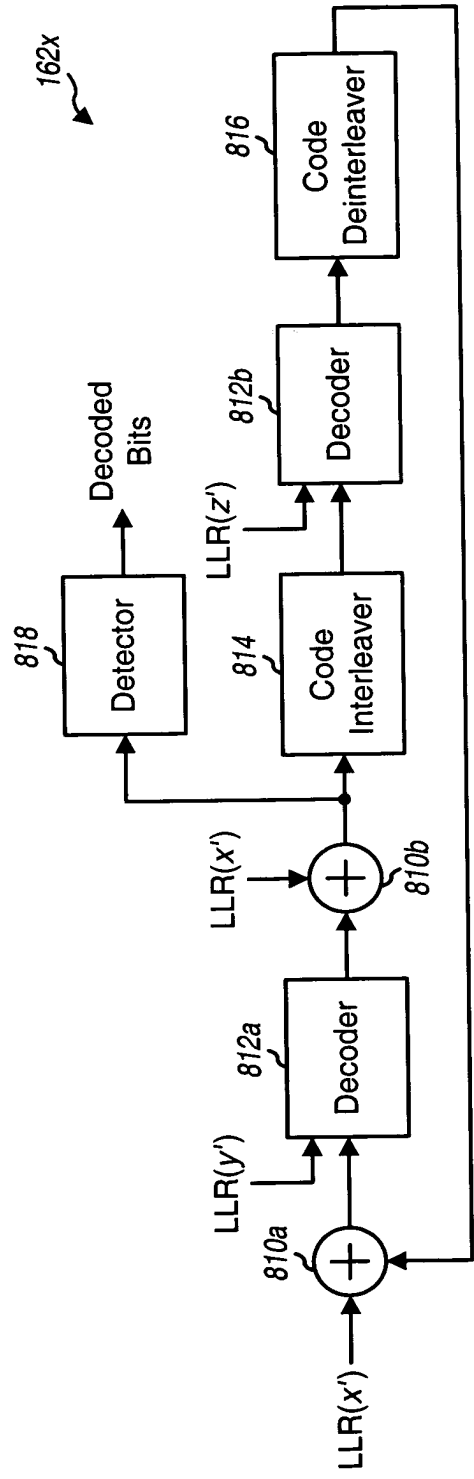
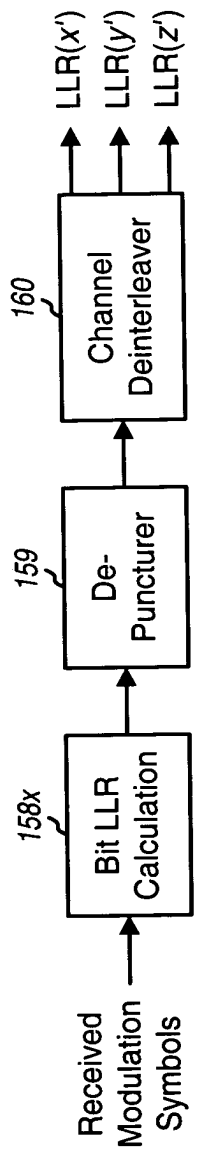


FIG. 8